

Spec New

10/7/7, 946
20040099936

CLAIMS

Supported
LW, D/H
Abstract calls
along with unit

We claim:

1. A method of forming an integrated chip package, comprising the steps of:
- providing a first substrate and a second substrate, each having conductive pads thereon;
- applying a mask to at least one of the first and second substrates, wherein the mask has a plurality of non-circular openings ^{etch} having a first dimension and a second dimension, such that the conductive pads are not covered by the mask in the direction of the first dimension and partially covered by the mask in the direction of the second dimension, and
- providing a reflowable material between the conductive pads of the first and second substrates.

Conflicts
w/ Spec p. 7
Delete

2. The method of claim 1, wherein the first dimension of the elongated non-circular openings is greater than the second dimension of the non-circular openings.

3. The method of claim 1, wherein the first dimension of the non-circular openings is selectively oriented in the direction of highest stress for each interconnection formed from the reflowable material within the integrated chip package.

6, 774, 474
11/10/99

1 4. The method of claim 1, wherein the non-circular openings of
2 the mask are elliptical.

1 5. The method of claim 1, wherein the conductive pads are
2 circular.

1 6. The method of claim 5, wherein the conductive pads are
2 copper.

1 7. The method of claim 1, wherein the mask comprises a non-
2 wettable material.

1 8. The method of claim 7, wherein the mask comprises an epoxy. 103

1 9. The method of claim 1, wherein the first substrate is a chip
2 carrier.

1 10. The method of claim 1, wherein the second substrate is a
2 printed circuit board.

1 11. The method of claim 1, wherein the reflowable material is
2 solder.

1 12. The method of claim 1, wherein a plurality of traces are
2 mounted between the non-circular openings of the mask.

1 13. The method of claim 1, wherein the integrated chip package
2 is a Ball Grid Array package.

1 14. An integrated chip package comprising:
2 a first substrate and a second substrate, wherein at least
3 one of the first and second substrates includes a plurality of
4 partially captured pads; and
5 a plurality of interconnections between the first and second
6 substrates.

1 15. The integrated chip package of claim 14, wherein the
2 plurality of partially captured pads are formed by a mask having
3 elongated non-circular mask openings.

1 16. The integrated chip package of claim 15, wherein the
2 elongated non-circular mask openings have a first dimension and a
3 second dimension.